REMARKS

Claims 1-20 remain pending. Applicants understand the previous 102 and 103 rejections have been overcome.

35 U.S.C. Section 102 Rejections

Paragraph 3 of the above referenced Office Action rejects independent Claims 1, 9, and 18 as being anticipated by Moreno (US 6,678,795). As such, Applicants respectfully traverse and assert that the independent Claims 1, 9, and 18 are not anticipated or rendered obvious by Moreno.

Applicants direct the Examiner to Claim 9 which recites in part (emphasis added):

> a cache memory coupled to the prefetch unit, wherein the prefetch unit uses a bit vector to predictively load target cache lines from the system memory into the cache memory to reduce an access latency of the processor, and wherein the target cache lines are indicated by the stream type access pattern identified by the trackers.

Independent Claim 1 and 18 recite distinguishing limitations similar to those recited in Claim 9.

Applicants wish to remind the Examiner that "a claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." Verdegaal Bros v. Union Oil Co. of California, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). Applicants point out that paragraph 5 of the above

reference Office Action states that Moreno does not specifically teach that these accesses are consecutive (Page 7). Further, Applicants point out that the previous Office Action (mailed 12/18/2006) states Moreno does not specifically disclose that the order of previous accesses to the two cache lines was not interrupted by other cache line accesses (Page 4).

Applicants further point out that "to establish inherency, the extrinsic evidence 'must make clear that the missing descriptive matter is necessarily present in the thing described in the reference, and that it would be so recognized by persons of ordinary skill. Inherency, however, may not be established by probabilities or possibilities. The mere fact that a certain thing may result from a given set of circumstances is not sufficient.' " In re Robertson, 169 F.3d 743, 745, 49 USPQ2d 1949, 1950-51 (Fed. Cir. 1999).

"In relying upon the theory of inherency, the examiner must provide a basis in fact and/or technical reasoning to reasonably support the determination that the allegedly inherent characteristic necessarily flows from the teachings of the applied prior art." Ex parte Levy, 17 USPQ2d 1461, 1464 (Bd. Pat. App. & Inter. 1990). As such, Applicants respectfully invite the Examiner to introduce extrinsic evidence to establish the alleged inherency or to kindly withdraw the rejections. Thus, the cited reference,

Moreno, as discussed above fails to expressly or inherently disclose the stream type access, as claimed.

Moreover, Applicants respectfully assert that the cite portions of Moreno relied upon to teach stream type access teach away from the claimed embodiments of the present invention and therefore do not render Claim 9 obvious within the meaning of 35 U.S.C. 103(a). Applicants point out the cited portions of Moreno describe prefetching of arbitrary lines within a page, which do not need to exhibit any pattern (Col 2, lines 1-2). Applicants point out that stream type access may exhibit a pattern and embodiments as recited in Claim 9 predictively load target cache lines based on stream type access pattern as claimed. Applicants further point out that the cited portions of Moreno describe that for each cache line whose bit is set to 1 in the PUM entry, the PMU engine generates a prefetch request and sends to it to the cache controller (Col 6, lines 60-63). Applicants point out that generating prefetch requests based solely on each cache line bit set to 1 results in each request being based any access pattern which is substantially different from stream type access as claimed. Thus, Applicants respectfully submit that Moreno actually teaches away from predictively loading target cache lines based on stream type access as claimed and therefore Moreno does not render the present invention as recited in Claim 9 obvious within the meaning of 35 U.S.C. 103(a).

Accordingly, Applicants resentfully asset that Moreno does not anticipate Claim 9 within the meaning of 35 U.S.C. §102(e) nor does Moreno render Claim 9 obvious within the meaning of 35 U.S.C. §103(a). Independent Claims 1 and 18 are patentable for similar reasons. Dependent claims are patentable by virtue of their dependency.

35 U.S.C. Section 103 Rejections

Paragraph 5 of the above referenced Office Action rejects dependent Claims 4, 12, and 20 as being rendered obvious by Moreno (US 6,678,795). As such, Applicants respectfully assert that Claims 4, 12 and 20 are not rendered obvious by Moreno. For the reasons stated above, Applicants respectfully assert that independents Claim 1, 9, and 18 are allowable over Moreno.

Claims 16, 17, and 19 stand rejected as being unpatentable over Moreno in view of Bittel (US 6,820,173), Microsoft Computer Dictionary, and Brooks (US 6,081,868) respectively.

Concerning Claim 16, the rejection relies on Bittel teaching a prefetch apparatus comprising a prefetch unit and a cache memory within the prefetech unit. Applicants point out that embodiments of the present

invention have a prefetch unit is configured to observe access by a CPU to system memory and L1 and L2 caches. In contrast, Applicants point out that the prefetcher in the northbridge of Bittel is located between the DRAM and the processor and is coupled to the processor by the system bus (Figure 2). Therefore, Applicants respectfully assert that Bittel teaches away from the present invention because Bittel teaches a prefetch unit not configured or coupled to obverse access to L1 and L2 caches. Therefore, Applicants respectfully assert that the embodiments of the present invention as recited in Claim 16 are not rendered obvious by the combination of Moreno and Bittel within the meaning of 35 U.S.C. 103(a).

Concerning Claim 17, the rejection relies on the Microsoft computer dictionary (hereinafter Microsoft) teaching a typical L2 cache has bigger capacity than a typical L1 and therefore it would have been obvious to one ordinarily skilled in the art to make Moreno's cache memory a L2 cache instead of a L1 cache in order to have larger caching capacity. To the extent that Mircosoft dictionary may mention than an i486 processor has typically 8KB of cache and an i486 processor typically has 128KB of cache, Applicants respectfully assert that the Mircosoft computer dictionary does not teach or suggest that an L2 cache is typically bigger in capacity than an L1. That is, Applicants point out that Microsoft only describes that typical cache size of a specific processor, the i486. Further, Applicants can find no mention or

suggestion in Mircosoft that L2 cache is required to be larger than L1 cache memory. Applicants respectfully assert that it would not have been obvious to one of ordinary skilled in the art to make Moreno's cache memory a L2 cache instead of a L1 cache in order to have a larger caching capacity. Therefore, Applicants respectfully assert that the embodiments of the present invention as recited in Claim 17 are not rendered obvious by the combination of Moreno and Microsoft within the meaning of 35 U.S.C. 103(a).

For the reasons stated above, Applicants respectfully assert that independent Claim 9, from which Claims 16 and 17 depend, independent Claim 18, from which Claim 19 depends are allowable over Moreno. In addition, Applicants respectfully assert that Bittel, Microsoft Computer Dictionary, and Brooks, respectively, do not remedy the short comings of Moreno. Therefore, Applicants respectfully submit that Claims 16, 17, and 19 are allowable over Moreno in view of Bittel, Microsoft Computer Dictionary, and Brooks, respectively, as being dependent on allowable base claims.

CONCLUSION

The Examiner is urged to contact Applicants' undersigned representative if the Examiner believes such action would expedite resolution of the present Application. Please charge any additional fees or apply any credits to our PTO deposit account number: 50-4160.

Respectfully submitted,
MURABITO, HAO & BARNES

Dated: 2/29, 2008

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I hereby certify that this correspondence is being electronically transmitted to the USPTO via EFS on the date shown below:

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